LISTING OF CLAIMS

1. (Original) A method comprising:

reviewing a first branching behavior of a first previous set of branching instructions executed by a processor;

reviewing multiple traces that have a same beginning instruction; and

selecting a trace from among the multiple traces based on the branching behavior of the first previous set of branching instructions.

2. (Original) The method of claim 1, further comprising:

selecting the trace from among the multiple traces that has a second branching behavior of a second previous set of branching instructions that matches the first branching behavior of the first previous set of branching instructions.

3. (Original) The method of claim 1, further comprising generating a new trace if a divergence occurs in a pre-determined location in the trace.

4. (Previously Presented) The method of claim 3, further comprising determining, based on which instruction within a block of instructions creates the branch, whether the new trace is generated.

5. (Previously Presented) The method of claim 3, further comprising determining, based on which block of instructions the branch occurs in, whether an alternate trace is generated.

6. (Original) A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor to implement a method for processing data, the method comprising:

reviewing a first branching behavior of a first previous set of branching instructions executed by a processor;

reviewing multiple traces that have a same beginning instruction; and

selecting a trace from among the multiple traces based on the branching behavior of the first previous set of branching instructions.

7. (Original) The set of instructions of claim 6, further comprising:

selecting the trace from among the multiple traces that has a second branching behavior of a second previous set of branching instructions that matches the first branching behavior of the first previous set of branching instructions.

8. (Original) The set of instructions of claim 6, further comprising generating a new trace if a divergence occurs in a pre-determined location in the trace.

9. (Previously Presented) The set of instructions of claim 8, further comprising determining, based on which instruction within a block of instructions creates the branch, whether the new trace is generated.

10. (Previously Presented) The set of instructions of claim 8, further comprising

determining, based on which block of instructions the branch occurs in, whether an alternate trace is generated.

11. (Original) A processor comprising:

a branch predictor to review a first branching behavior of a first previous set of branching instructions executed by a processor;

a trace cache to store multiple traces that have a same beginning instruction; and

a fetching mechanism to retrieve a trace from among the multiple traces based on the first branching behavior of the previous set of branching instructions.

12. (Original) The processor of claim 11, wherein the fetching mechanism is to select the trace from among the multiple traces that has a second branching behavior of a second previous set of branching instructions that matches the first branching behavior of the first previous set of branching instructions.

13. (Previously Presented) The processor of claim 11, further comprising a processing core to execute the trace and to generate a new trace if a divergence occurs in a pre-determined location in the trace.

14. (Original) The processor of claim 13, wherein whether the new trace is generated is based on which instruction within a block of instructions creates the branch.

15. (Previously Presented) The processor of claim 13, wherein whether an alternate trace is

generated is based on which block of instructions the branch occurs in.

16. (Original) A system comprising:

a memory to store a set of instructions;

a processor coupled to the memory to execute the set of instructions, the processor with a branch predictor to review a first branching behavior of a first previous set of branching instructions executed by a processor, a trace cache to store multiple traces that have a same beginning instruction, and a fetching mechanism to retrieve a trace from among the multiple traces based on the first branching behavior of the previous set of branching instructions.

17. (Original) The system of claim 16, wherein the fetching mechanism is to select the trace from among the multiple traces that has a second branching behavior of a second previous set of branching instructions that matches the first branching behavior of the first previous set of branching instructions.

18. (Original) The system of claim 16, further comprising a processing core to execute the trace and to generate a new trace if a divergence occurs in a pre-determined location in the trace.

19. (Original) The system of claim 18, wherein whether the new trace is generated is based on which instruction within a block of instructions creates the branch.

20. (Previously Presented) The system of claim 18, wherein whether an alternate trace is generated is based on which block of instructions the branch occurs in.